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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/777,897	02/07/2001	Nobutaka Taniguchi	100353-00039	4758
7590 05/21/2004				
ARENT FOX KINTNER PLOTKIN & KAHN, PLLC 1050 Connecticut Avenue, N.W., Suite 600 Washington, DC 20036-5339			EXAMINER NGUYEN, LINH M	
			ART UNIT 2816	PAPER NUMBER

DATE MAILED: 05/21/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	<b>Applicati n No.</b> 09/777,897	<b>Applicant(s)</b> TANIGUCHI, NOBUTAKA	
	<b>Examiner</b> Linh M. Nguyen	<b>Art Unit</b> 2816	

**-- The MAILING DATE of this communication app ars on the cover sheet with the correspondenc address --**

**Peri d f r Reply**

**A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.**

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 18 March 2004.
- 2a) ☐ This action is **FINAL**.                      2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disp sition of Claims**

- 4) ☒ Claim(s) 1-8 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-8 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 07 February 2001 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Pri rity under 35 U.S.C. § 119**

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All    b) ☐ Some \* c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |  |   |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892)   | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                                   | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)             |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____  |

### **DETAILED ACTION**

This Office Action is a response to the Applicant's amendment filed 03/18/2004. Claims 1-8 are currently presented in the instant application.

#### ***Drawings Objection***

1. The drawings are objected to because of the following minor informalities:

Fig. 5, box 22 change "ditection" to -detection--.

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Appropriate correction is required.

#### ***Claim Objections***

2. Claim 3 is objected to because of the following informalities:

Line 3, change "input second" to -output second--;

Line 6, change "an' (in front of "output") to -the--.

Appropriate correction is required.

#### ***Claim Rejections - 35 USC § 112***

3. The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

4. Claims 3-8 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

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As to claim 3, the recitation “*the adjusting of said delay at an initial stage of the adjusting is to increase said delay irrespective of said comparison when starting the step of adjusting of said delay*”, in lines 14-15, is not described in the specification. Such limitation makes the claimed invention unclear, and as such, it creates difficulty in distinguishing the claimed invention with the prior art. A full explanation is required to clarify the claimed invention.

As to claims 4 and 6, the recitation “*the step of delaying at an initial stage of adjustment is to increase the delay time irrespective of said comparison when starting the delay time adjustment*”, in lines 14-15 of claim 4, lines 15-16 of claim 6, is not described in the specification. Such limitation makes the claimed invention unclear, and as such, it creates difficulty in distinguishing the claimed invention with the prior art. A full explanation is required to clarify the claimed invention.

As to claim 5, the recitation “*delaying means for increasing a delay time of said phase of said output signal irrespective of said detection of phase difference*”, in lines 7-8 of claim 5, is not described in the specification. Such limitation makes the claimed invention unclear, and as such, it creates difficulty in distinguishing the claimed invention with the prior art. A full explanation is required to clarify the claimed invention.

As to claim 7, the recitation “*the steps of delaying at an initial stage of adjustment is to increase the delay time irrespective of said comparison when starting the delay time adjustment*”, in lines 16-18, is not described in the specification. Such limitation makes the claimed invention unclear, and as such, it creates difficulty in distinguishing the claimed invention with the prior art. A full explanation is required to clarify the claimed invention.

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Claim 8 is also rejected under 35 U.S.C. 112, first paragraph, because of its dependency on claim 7.

5. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. Claims 3-8 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

As to claim 3, the term “*irrespective*” in “*the adjusting of said delay at an initial state of adjusting is to increase irrespective of said comparison when starting the step of adjusting of said delay*”, in lines 14-15, renders the claim indefinite as it is unclear how delaying is irrespective of the comparison at initial stage of adjustment. As shown in figure 5 of the claimed invention, the delay is performed (*via [24]*) after the process of comparison (*performed by [8]*). Clarification is required.

As to claims 4 and 6, the term “*irrespective*” in “*the step of delaying at an initial stage of adjustment is to increase the delay time irrespective of said comparison when starting the delay time adjustment*”, in lines 14-15 of claim 4, lines 15-16 of claim 6, renders the claim indefinite as it is unclear how delaying is irrespective of the comparison at an initial stage of adjustment. As shown in figure 5 of the claimed invention, the delay is performed (*via [24]*) after the process of comparison (*performed by [8]*). Clarification is required.

As to claim 5, the term “*irrespective*” in “*delaying means for increasing a delay time of said phase of said output signal irrespective of said detection of phase difference*”, in lines 7-8,

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renders the claim indefinite as it is unclear how delaying is irrespective of the phase difference.

As shown in figure 5 of the claimed invention, the delay is performed (*via [24]*) after the process of comparison (*performed by [8]*). Clarification is required.

As to claim 7, the term “*irrespective*” in “*the steps of delaying at an initial stage of adjustment is to increase the delay time irrespective of said comparison when starting the delay time adjustment*”, in lines 16-18, renders the claim indefinite as it is unclear how delaying is irrespective of the comparison when starting time adjustment is performed. As shown in figure 5 of the claimed invention, the delay is performed (*via [24]*) after the process of comparison (*performed by [8]*). Clarification is required.

Claim 8 is also rejected under 35 U.S.C. 112, second paragraph, because of its dependency on claim 7.

### ***Claim Rejections - 35 USC § 102***

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000.

Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

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8. Claims 1-2 and 5 are rejected under 35 U.S.C. 102(e) as being anticipated by Yada et al. (U.S. Patent No. 6,266,294).

With respect to claim 1, Yada et al. discloses, in Fig. 3, a delay time adjusting circuit with a corresponding method of adjusting a delay time of an input signal [I-CLK] so that a phase of the input signal and a phase of an output signal [DLL-CLK] match each other, based on a comparison between phases of the input signal and the output signal, the method comprises the steps of a) comparing [23] phases of the output signal and the input signal with each other, and b) starting [24] an increase of the delay time at any time when a phase difference is detected in the step of comparing.

With respect to claim 2, AAPA, Fig. 1, discloses that the method further comprises a step of producing the output signal by delaying the input signal by a DLL circuit [11].

With respect to claim 5, as best understood, Yada et al. discloses, in Fig. 3, a delay time adjusting circuit for adjusting a delay time of an input signal [I-CLK] so that a phase of the input signal and a phase of an output signal [DLL-CLK] match each other between phases based on a comparison of the input signal and the output signal, the circuit comprising a) detecting means [23] for detecting a phase difference between the phase of the input signal and the phase of the output signal; and b) delaying means [20,21] for increasing a delay time of the phase of the output signal irrespective of said detection based on the phase difference when the phase difference becomes N periods, where N is an integer other than zero.

*Allowable Subject Matter*

9. Claim 3 would be allowed a) if corrected to overcome the objection set forth in this office action and b) if rewritten or amended to overcome the rejection(s) under 35 U.S.C. 112, 1<sup>st</sup> and 2<sup>nd</sup> paragraph, set forth in this office action.

10. Claims 4 and 6-8 would be allowable if rewritten or amended to overcome the rejection(s) under 35 U.S.C. 112, 1<sup>st</sup> and 2<sup>nd</sup> paragraph, set forth in this office action.

11. The following is a statement of reasons for the indication of allowable subject matter:

The closest prior art on record does not show or fairly suggest:

a) A delay time adjusting method including a step of adjusting a delay time of the input first periodic signal so that a phase of the input first periodic signal and a phase of the output second periodic signal match within a predetermined tolerance, in combination with the remaining claimed limitations, as called for in claim 3;

b) A delay time adjusting method including a second step of increasing the delay time to adjust a phase of an output second periodic signal so that, when the phase of a predetermined rising edge is judged to be behind the phase of the first rising edge in the first step, the phase of the predetermined rising edge and a phase of a second rising edge of the input first periodic signal match each other, the second rising edge being one period behind the first rising edge, in combination with the remaining claimed limitations, as called for in claim 4;

c) A delay time adjusting circuit for adjusting a delay time of an input periodic signal including a delaying means for adjusting said delay time so that, when the phase of a predetermined rising edge of an output second periodic signal is judged to be behind the phase of the predetermined rising edge of the input first periodic signal by a judging means, the



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predetermined rising edge of the output second periodic signal matches a rising edge of the input first periodic signal, a phase of the rising edge being behind and nearest to the phase of the predetermined rising edge of the output second periodic signal, in combination with the remaining claimed limitations, as called for in claim 6; and

d) A delay time adjusting circuit for adjusting a delay time of an input first periodic signal including a adjusting means for controlling a delaying means so that, when the phase of a predetermined rising edge is judged to be behind the phase of a first rising edge by a phase-detecting means, the delaying means delays the phase of an output second periodic signal until the phase of the predetermined rising edge and a phase of a second rising edge of an input first periodic signal match each other, the second rising edge being one period behind the first rising edge, in combination with the remaining claimed limitations, as called for in claim 7.

### ***Remarks***

12. With respect to the Applicant's arguments on claim 3, at page 8, second paragraphs, the Applicants state that *"the adjusting of said delay at an initial stage of the adjusting is to increase the delay irrespective of said comparison when starting the step of adjusting of said delay...is enabled in the specification at page 15, line 12 to page 16, line 32."* The examiner disagrees with the statement. Regarding Fig.5 of the claimed invention, phase comparator [8] has to provide signal [out] to state detection circuit [22] and state judgment circuit [20] in order to adjust the delay time by TD, (see page 13, lines 16-35) and page 16, lines 20-23.

With respect to the Applicant's arguments on claims 4 and 6, last paragraph of page 8 bridging page 9, the Applicants state that the limitation *"the step of delaying at an initial stage of the adjustment is to increase the delay time irrespective of said comparison when starting the*

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*delay time adjustment*". This amendment is also enabled in the specification at page 15, line 12 to page 16, line 33. "". The examiner disagrees with the statement. Regarding Fig.5 of the claimed invention, phase comparator [8] has to provide signal [out] to state detection circuit [22] and state judgment circuit [20] in order to adjust the delay time by TD, (see page 13, lines 16-35) and page 16, lines 20-23.

With respect to the Applicant's arguments on claims 7 and 8, first full paragraph of page 9, the Applicants state that "*the step of delaying at an initial stage of the adjustment is to increase the delay time irrespective of said comparison when starting the delay time adjustment*". Support for ... in the specification at page 15, line 12 to page 16, line 33." The examiner disagrees with the statement. Regarding Fig.5 of the claimed invention, phase comparator [8] has to provide signal [out] to state detection circuit [22] and state judgment circuit [20] in order to adjust the delay time by TD, (see page 13, lines 16-35) and page 16, lines 20-23.

With respect to the Applicant's arguments on claims 3, 4, 6 and 7, second and third paragraphs at page 10, see similar responses in the above three paragraphs.

### ***Inquiry***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Linh M. Nguyen whose telephone number is (571) 272-1749. The examiner can normally be reached on Alternate Mon, Tuesday - Friday from 7:00 to 4:30.

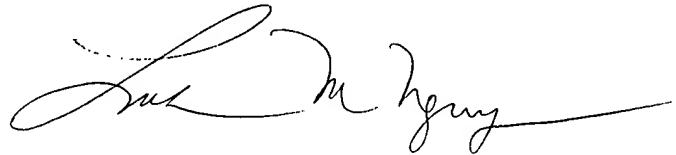
If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy P Callahan can be reached on (571) 272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Linh M. Nguyen  
Examiner  
Art Unit 2816

LMN

A handwritten signature in black ink, appearing to read 'Linh M. Nguyen', with a long horizontal flourish extending to the right.